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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/288,263	04/08/1999	HIROYUKI WAKI	NAK1-BG55	7236

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EXAMINER	
LAFORGIA, CHRISTIAN A	
ART UNIT	PAPER NUMBER
2131	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/288,263	WAKI ET AL.	
	Examiner	Art Unit	
	Christian La Forgia	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30,39-44,52 and 53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30,39-44,52 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 1/17/03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 26 October 2004 has been noted and made of record.

2. Claims 30, 39-44, 52, and 53 have been presented for examination.

Response to Arguments

3. Applicant's arguments filed 26 October 2004 have been fully considered but they are not persuasive.

4. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

5. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features, such as executing of the generated instruction sequence without specifying or converting to a target system, upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Applicant does NOT claim the instruction sequence is executed without converting to a target system (i.e. interpreted), therefore the rejection is upheld as the Examiner is giving the claims their broadest reasonable interpretation in light of the specification without reading limitations from the specification into the claim language. See *E-Pass Techs., Inc. v. 3Com Corp.*, 343 F.3d 1364, 1369, 67 USPQ2d 1947, 1950 (Fed. Cir. 2003), see *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997), see § MPEP 2106.

6. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features, such as not requiring recreation or generation of the basic block by the virtual machine during execution, upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

7.. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features, such as not having to divide the basic blocks during runtime activities, upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

See further rejections that follow.

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 30, 39-44, 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Java!**, by Tim Ritchey, hereinafter Ritchey, in view of **Compilers: Principles, Techniques, and Tools**, by Alfred V. Aho et al., hereinafter Aho.

10. As per claims 30, 39, 52, and 53, Ritchey teaches a data storage comprising:

generating a virtual machine instruction sequence by compiler to be executed by a virtual machine, see page 53, "Finally, the Javac compiler enables developers to compile for the Java

Virtual Machine, providing applications which will run on any system for which the browser or interpreter have been ported," page 326, "The Java system begins with the Java code developed by a programmer. This code is fed to a compiler which generates the Java bytecode for the virtual machine", see page 328, "It is the Java Virtual Machine for which the Java compiler compiles the source code";

transmitting the instruction block to the virtual machine, see page 331, Figure 14.1;

storing the instruction block in the virtual machine, see pages 336-342, specifically Sections entitled "The Instruction Set," "The Registers," "The Java Stack," "Local Variables," "Execution Environment," "Operand Stack," and "The Memory Area."

11. For a better illustration of a java compiler and transmitting the instruction block to the virtual machine please refer to pages 162 and 163, specifically Figures 9.1 and 9.2, of **Java Developer's Reference**, by Mike Cohn et al.

12. Ritchey does not teach dividing the virtual machine instruction sequence into basic blocks each corresponding to an instruction block, see pages 336-337, "The instruction set for the JVM [Java Virtual Machine] is exactly equivalent to the instruction set for a CPU," for dividing the virtual machine instruction sequence into sets corresponding to instruction sets for a CPU.

13. Aho discloses dividing the machine instruction sequence into basic blocks each corresponding to an instruction block, see pages 529-530, Algorithm 9.1, Example 9.2, and Figures 9.7 and 9.8.

14. Aho defines a basic block as a sequence of consecutive statements in which flow of control enters at the beginning and leaves at the end without halt or possibility of branching

except at the end. Therefore, Aho teaches wherein the format of the instruction block includes an identifier area for storing an identifier that specifies a start position of the instruction block, see page 529, Aho's discussion of determining of *leaders*. According to Aho's definition provided above, the next part of the basic block would be a non-branch instruction area for storing non-branch instructions belonging to the corresponding basic block. Still going by Aho's definition of a basic block, the branch instruction area would have to be at the end of the basic block thereby designating the next leader or basic block. Aho further discloses storing branch identifiers on pages 546-552. This is further based on the definition of a basic block as defined in column 2, lines 15-23 of U.S. Patent No. 6,044,222 to Simons et al., which states:

> A basic block is a contiguous sequence of instructions such that control flow can only enter at the first instruction and leave at the last instruction. Basic blocks have the characteristic that if one of the instructions is ever executed by the program, all the instructions in the basic block will be executed (assuming that no exceptions occur). A basic block typically starts at a branch label and is typically terminated by some sort of a branch instruction.

Graphical representations of basic blocks can be found in Figures 1-6, 10, 12, 15-21, 23a, 23b, 23c, 26a, and 28b of U.S. Patent No. 5,923,883 to Tanaka et al.

15. It would have been obvious to one of ordinary skill in the art at the time the invention was made for the compiler to divide the virtual machine instruction sequence into basic blocks each corresponding to an instruction block, since Aho states on page 530, section 9.4 that such a modification would be useful for optimizing the code in an effort to reduce the overall running time or space required for the final program.

16. Regarding claim 40, Ritchey teaches wherein the identifier of the instruction block is address related information in the virtual machine instruction sequence, see page 330.

17. With regards to claim 41, Aho teaches wherein the address related information is one of absolute address, relative address, and offset address, see pages 519 and 520.

18. Regarding claim 42, Ritchey discloses wherein whether each virtual machine instruction is positioned at a start position of the basic block is indicated by an address in the virtual machine instruction sequence to which the virtual machine instruction is allocated, see page 330;

a virtual machine instruction at the start position of the basic block being allocated to a specific address in the virtual machine instruction sequence, see page 330, and

a virtual machine instruction at other than the start position of the basic block being allocated to an address other than the specific address, see page 330.

19. Regarding claim 43, Ritchey teaches an identifying unit for storing identification information which indicates if the virtual machine instruction is positioned at a start position of the basic block, see page 339, the program counter;

an operation specifying unit for specifying an operation to be executed by the virtual machine, see pages 336-338, "The Instruction Set."

20. Regarding claim 44, Aho teaches the basic blocks, see pages 528-533;

identification tags, each designates an address related information of the virtual machine instruction at a start position of the basic block; attachment of the tag indicating if the virtual machine instruction corresponding to the identification tag is positioned at the start position of the basic block, pages 546-533.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

22. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian La Forgia whose telephone number is (571) 272-3792. The examiner can normally be reached on Monday thru Thursday 7-5.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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